WHAT IS CLAIMED IS:

1. A method for manufacturing a phase-change memory device comprising the steps of:

(a) forming a lower electrode, at least a part of the lateral surface of the lower electrode being surrounded by a lower dielectric layer, at least a part of the top surface of the lower electrode being exposed;

(b) forming a thin dielectric layer so that the exposed part of the top surface of the lower electrode and the top surface of the lower dielectric layer are covered;

(c) forming a mask pattern on the thin dielectric layer;

(d) forming a pore in the thin dielectric layer, having smaller area than the exposed part of the top surface of the lower electrode and aligned to the exposed part of the top surface of the lower electrode, by etching the thin dielectric layer with the mask pattern;

(e) removing the mask pattern; and

(f) depositing a phase-change material on the thin dielectric layer to fill the pore.

2. The method as set forth in claim 1, wherein the step (a) comprises the steps of:

forming a recessed part having a tapered sidewall in the lower dielectric layer;

depositing the lower electrode material to fill the recessed part; and

planarizing the lower electrode material so that the top surface of the part of the lower dielectric layer where the recessed part is not formed is exposed.

3. The method as set forth in claim 1, wherein the

step (c) comprises the steps of:

coating a polymeric resist film; and

patterning on the polymeric resist film using an imprinting stamp having protrusions, the ends of which have width below than 1 micrometer.

4. A method for manufacturing a phase-change memory device comprising the steps of:

(a) forming a lower electrode, at least a part of the lateral surface of the lower electrode being surrounded by a lower dielectric layer, at least a part of the top surface of the lower electrode being exposed;

(b) forming a thin dielectric layer so that the exposed part of the top surface of the lower electrode and the top surface of the lower dielectric layer are covered;

(c) forming a mask pattern on the thin dielectric layer;

(d) forming a damaged spot in the thin dielectric layer, having smaller area than the exposed part of the top surface of the lower electrode and aligned to the exposed part of the top surface of the lower electrode, to provide a micro current path;

(e) removing the mask pattern; and

(f) depositing a phase-change material on the thin dielectric layer including the damaged spot.

5. The method as set forth in claim 4, wherein the step (a) comprises the steps of:

forming a recessed part having a tapered sidewall in the lower dielectric layer;

depositing the lower electrode material to fill the recessed part; and

planarizing the lower electrode material so that the

top surface of the part of the lower dielectric layer where the recessed part is not formed is exposed.

6. The method as set forth in claim 4, wherein the step (c) comprises the steps of:

coating a polymeric resist film; and

patterning on the polymeric resist film using an imprinting stamp having protrusions, the ends of which have width below than 1 micrometer.

7. The method as set forth in claim 4, wherein the step (d) comprises the step of:

exposing unmasked area on the thin dielectric layer to a plasma, in order to form the damaged spot.

8. The method as set forth in claim 4, wherein the step (d) comprises the step of:

exposing unmasked area on the thin dielectric layer to a UV light, in order to form the damaged spot.

9. The method as set forth in claim 4, wherein the step (d) comprises the step of:

exposing unmasked area on the thin dielectric layer to an ion beam, in order to form the damaged spot.

10. A method for manufacturing a phase-change memory device comprising the steps of:

(a) forming a lower phase-change resistor, at least a part of the lateral surface of the phase-change resistor being surrounded by a lower dielectric layer, at least a part of the top surface of the lower phase-change resistor being exposed;

(b) forming a thin dielectric layer so that the

exposed part of the top surface of the lower phase-change resistor and the top surface of the lower dielectric layer are covered;

(c) forming a mask pattern on the thin dielectric layer;

(d) forming a pore in the thin dielectric layer, having smaller area than the exposed part of the top surface of the lower phase-change resistor and aligned to the exposed part of the top surface of the lower phase-change resistor, by etching the thin dielectric layer with the mask pattern; and

(e) removing the mask pattern.

11. The method as set forth in claim 10, further comprising the step of:

(f) depositing an electrode material on the thin dielectric layer to fill the pore.

12. The method as set forth in claim 10, further comprising the step of:

(f) depositing a phase-change material on the thin dielectric layer to fill the pore and form an upper phase-change resistor.

13. A method for manufacturing a phase-change memory device comprising the steps of:

(a) forming a lower phase-change resistor, at least a part of the lateral surface of the phase-change resistor being surrounded by a lower dielectric layer, at least a part of the top surface of the lower phase-change resistor being exposed;

(b) forming a thin dielectric layer so that the exposed part of the top surface of the lower phase-change

resistor and the top surface of the lower dielectric layer are covered;

(c) forming a mask pattern on the thin dielectric layer;

(d) forming a damaged spot in the thin dielectric layer, having smaller area than the exposed part of the top surface of the lower phase-change resistor and aligned to the exposed part of the top surface of the lower phase-change resistor, to provide a micro current path; and

(e) removing the mask pattern.

14. The method as set forth in claim 13, further comprising the step of:

(f) depositing an electrode material on the thin dielectric layer including the damaged spot.

15. The method as set forth in claim 13, further comprising the step of:

(f) depositing a phase-change material on the thin dielectric layer including the damaged spot and form an upper phase-change resistor.

16. A phase-change memory device comprising:

(a) a lower dielectric layer;

(b) a lower electrode, at least a part of the lateral surface of the lower electrode being surrounded by the lower dielectric layer;

(c) a thin dielectric layer including a pore having smaller area than the top surface of the lower electrode, aligned to the top surface of the lower electrode and extending to the top surface of the lower electrode; and

(d) a phase-change resistor filling the pore and formed on the thin dielectric layer.

17. The phase-change memory device as set forth in claim 16, wherein the lower electrode is filling a recessed part having a tapered sidewall in the lower dielectric layer so that the top surface area of the lower electrode is larger than the bottom surface area; and

wherein large lithographic margin is provided owing to the large top surface area.

18. A phase-change memory device comprising:

(a) a lower dielectric layer;

(b) a lower electrode, at least a part of the lateral surface of the lower electrode being surrounded by the lower dielectric layer;

(c) a thin dielectric layer including a damaged spot having smaller area than the top surface of the lower electrode, aligned to the top surface of the lower electrode and providing a current path to the top surface of the lower electrode; and

(d) a phase-change resistor aligned to the damaged spot and formed on the thin dielectric layer.

19. The phase-change memory device as set forth in claim 18, wherein the lower electrode is filling a recessed part having a tapered sidewall in the lower dielectric layer so that the top surface area of the lower electrode is larger than the bottom surface area; and

wherein large lithographic margin is provided owing to the large top surface area.

20. A phase-change memory device comprising:

(a) a lower dielectric layer;

(b) a lower phase-change resistor, at least a part

of the lateral surface of the lower phase-change resistor being surrounded by the lower dielectric layer; and

(c) a thin dielectric layer including a pore having smaller area than the top surface of the lower phase-change resistor, aligned to the top surface of the lower phase-change resistor and extending to the top surface of the lower phase-change resistor.

21. The phase-change memory device as set forth in claim 20, further comprising:

(d) an upper electrode filling the pore and formed on the thin dielectric layer.

22. The phase-change memory device as set forth in claim 20, further comprising:

(d) an upper phase-change resistor filling the pore and formed on the thin dielectric layer.

23. A phase-change memory device comprising:

(a) a lower dielectric layer;

(b) a lower phase-change resistor, at least a part of the lateral surface of the lower phase-change resistor being surrounded by the lower dielectric layer; and

(c) a thin dielectric layer including a damaged spot having smaller area than the top surface of the lower phase-change resistor, aligned to the top surface of the lower phase-change resistor and providing a current path to the top surface of the lower phase-change resistor.

24. The phase-change memory device as set forth in claim 23, further comprising:

(d) an upper electrode aligned to the damaged spot and formed on the thin dielectric layer.

25. The phase-change memory device as set forth in claim 23, further comprising:

(d) an upper phase-change resistor aligned to the damaged spot and formed on the thin dielectric layer.